

Attorney's Docket No.: 10559-882001 / P17484  
Intel Corporation

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### Listing of Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Previously Presented) A system comprising:

a first apparatus to radiate an interference pattern of lines and spaces on a photoresist, the lines having a substantially equal first width and remaining unexposed to radiation, the spaces being exposed to radiation; and

a second apparatus to radiate selected areas of the photoresist, the selected areas exposing portions of the lines to radiation, wherein a pitch of the selected areas exposed by the second subsystem is at least one and a half times a pitch of the interference pattern; and

an alignment apparatus to align the selected areas radiated by the second apparatus with the interference pattern radiated by the first apparatus to trim and narrow the first width of at least some of the lines.

2. (Original) The system of Claim 1, wherein a second width of a feature formed by the second apparatus is equal to the first width of a line of the interference pattern.

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3. (Original) The system of Claim 1, wherein a second width of a feature formed by the second apparatus is less than the first width of a line of the interference pattern.

4. (Original) The system of Claim 1, wherein the second apparatus uses optical proximity correction (OPC) on a mask to adjust feature widths.

5. (Original) The system of Claim 1, wherein the first apparatus comprises a beamsplitter.

6. (Original) The system of Claim 1, wherein the first apparatus comprises a diffraction grating.

7. (Original) The system of Claim 1, wherein the second apparatus comprises a mask-based optical lithography tool.

8. (Original) The system of Claim 1, wherein the second apparatus comprises an electron beam lithography tool.

9. (Original) The system of Claim 1, wherein the second apparatus comprises a maskless optical lithography tool with a database.

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10. (Original) A method comprising:  
forming an interference pattern of non-exposed lines and  
exposed spaces on a photoresist, the lines having a first width;  
exposing a portion of at least one line to radiation to  
form features with a second width, the second width being less  
than the first width, wherein a pitch of the features is at  
least one and a half times a pitch of the interference pattern.

11. (Original) The method of Claim 10, wherein a pitch of  
the features is greater than one and a half times a pitch of the  
interference pattern.

12. (Original) The method of Claim 10, wherein the  
radiation has a pre-determined wavelength, the interference  
pattern approaching a pitch equal to the wavelength divided by  
two.

13. (Original) The method of Claim 10, further comprising  
generating a print mask from Boolean subtraction of (a) a final  
design layout for a given layer from (b) the interference  
pattern.

14.-24. (Canceled)

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25. (Previously Presented) A method comprising:  
using interference lithography to expose an interference pattern of non-exposed lines and exposed spaces on a photoresist, wherein the interference pattern has a first pitch; and

using a second lithography process to trim and narrow a width of at least some of the non-exposed lines by exposing portions of the non-exposed lines using a second exposure having a second pitch, wherein the second pitch is different from the first pitch.

26. (Previously Presented) The method of claim 25, wherein the second pitch is at least one and a half times the first pitch.

27. (Previously Presented) The method of claim 25, wherein using the second lithography process comprises using a lens-based lithography process.